REMARKS

Claims 23 through 32 are currently pending in the application.

Claims 23 and 25 have been amended. Reconsideration of the application is respectfully requested.

This amendment is in response to the Office Action of May 7, 2003.

Claims 23 through 32 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bol (U.S. Patent 5,269,877) in view of Yeh et al. (U.S. Patent 4,400,866) in further view of Brodie (U.S. Patent 5,063,327).

Applicant submits that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Bol teaches or suggests a process for making tip structures in conical or other shapes. (Col. 1, lines 44-45). The tip structures are produced on a substrate 10. Silicon is convenient but not necessary for the process. A 1.5-2.0 micron layer of amorphous silicon or polysilicon 12 with a surface 11 is deposited on substrate 10. (Col. 3, lines 15-19, FIG. 1). The amorphous silicon or polysilicon has a dopant concentration that is greatest at surface 11 and least at the interface between the amorphous silicon or polysilicon 12 and the substrate 10. (Col. 3, lines 20-25). Next, a nitride layer 16, 0.3-0.4 microns thick is deposited on the amorphous silicon or polysilicon 12. (Col. 3, lines 30-32). The next step is to pattern the nitride layer 16 and the amorphous silicon or polysilicon 12. This is done using a conventional photoresist process. (FIG. 4, Col. 3, lines 37-39). After etching, the amorphous silicon or polysilicon 12 has tapered sidewalls due to the higher dopant concentration, which speeds up the etching process. (FIG. 5, Col. 3, lines 42-45). The amorphous silicon or polysilicon 12 is next oxidized to grow oxide bumpers 20. (FIG. 6). Fastest growth of oxide bumpers occurs at areas of highest dopant

concentration. (Col. 3, lines 47-48, 53-55). Thus, oxide bumper 20 grows fastest and thickest near surface 11 of the amorphous silicon or polysilicon 12. Nitride layer 16 contributes to the final shape of oxide bumper 20. Because oxygen does not diffuse through the nitride layer 16, no oxide is grown on nitride layer 16. (Col. 3, lines 57-63). Fastest oxidation occurs just below interface 13 and decreases with decreasing dopant concentration. (FIG. 6, Col. 4, lines 4-6). The tip structure 22 includes base 24 and point 26. This tip structure 22 is formed as oxide bumper 20 grows. (Col. 4, lines 7-9). The final process step is removal of the oxide and nitride layers, leaving tip structure 22. Conventional process steps are used to remove the oxide and nitride layers. (Col. 4, lines 15-18).

Yeh teaches or suggests a structure for a high-speed VLSI self-aligned Schottky metal semi-conductor field effect transistor (SASMESFET) having a relatively high operating frequency and low series resistance predicated on controllable small structure geometries created by growing oxide bumper insulators on either side of the Schottky barrier. (Abstract). The structure 5 is formed on a substrate 10. (FIG. 1, Col. 3, lines 12-14). Substrate 10 is preferably a semi-insulating silicon that has been slightly P-doped with boron. Source and drain areas are implanted in substrate 10 at 90-1 and 90-2. (FIG. 1). A channel area has been implanted between source and drain areas 90-1 and 90-2 at 30'. Initial or source and drain substrate oxide layers have been grown on substrate 10 over the to be defined source and drain areas at 20"-1 and 20"-2. (Col. 3, lines 16-20). At the source and drain windows 110-1 and 110-2 platinum-silicide (PtSi) ohmic contacts 120-1 and 120-2 have been formed adjacent to the substrate 10. (Col. 3, lines 20-23). The PtSi contact 120-3 is a Schottky barrier for the Schottky gate area 70. (Col. 3, lines 23-25). Over the PtSi contacts a titanium-tungsten (TiW) layer 125 is deposited, followed by a layer of aluminum. (Col. 3, lines 25-27). Areas 135-1 and 135-2 are then etched down to the initial silicon dioxide layer 20"-1 and 20"-2. These etched down areas are formed to electrically separate the source contact/window area 110-1 from the gate area 70 and the drain contact/window area 110-2 from the gate area 70. (FIG. 1, Col. 3, lines 28-32). Insulators or oxide bumpers 80-1 and 80-2 are formed over the substrate 10 as adjuncts to the initial oxide layers 20"-1 and 20"-2 and are proximate to the Schottky gate area 70. (FIG. 1, Col. 3, lines 33-36). The spatial separation of source to gate 7-1 and drain to gate 7-2 can be varied by increasing

or decreasing the doping level as well as the thickness of the polysilicon layer 40' (FIG. 4f). The width of the oxide bumpers 80-1 and 80-2 is larger than the thickness of the oxidized silicon or initial silicon dioxide layers 20"-1 and 20"-2. (FIG. 3, Col. 4, lines 15-21).

Brodie teaches or suggests a flat panel display of the field emission cathode type. Each pixel of the display includes one base electrode 37 and three gates 38 which are orthogonally related to. (Col. 4, lines 41-45) The base electrode 37 is a layer strip 41 of conductive material applied to an insulating substrate. Such strip has electron emitting tips 43. (Col. 5, lines 1-2)

Applicant respectfully submits that regarding the presently claimed invention of independent claims 23, 25, 27, and 31, any cited prior art combination of Bol, Yeh et al., and Brodie does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention. The Applicant submits that there is no suggestion in the cited prior art or within the knowledge generally available to one of ordinary skill in the art for any combination thereof, the combination of the cited prior art does not teach or suggest all the claim limitations of the presently claimed invention, and any rejection of the presently claimed invention is based on impermissible hindsight based on the Applicant's disclosure, not the cited prior art.

First, Applicant submits that there is no suggestion in either the Bol reference or the Yeh et al. reference to combine or modify the references. Applicant submits that improper hindsight is being used to piece together parts of the prior art to create the Applicant's invention based solely upon Applicant's disclosure. The Bol reference is directed to the formation of tip microstructures in amorphous silicon or polysilicon layer *that has been deposited on a substrate.* Bol specifically refers to item 10 as being a substrate layer, while item 12 is a layer of amorphous silicon or polysilicon. (FIG. 1, Col. 3, lines 15-19). Bol is silent and does not teach or suggest forming tip microstructures directly from a single-layered substrate. Applicant respectfully submits that the claimed process by Bol for making a tip, as recited in Bol claim 1, includes a base substrate. Bol claim 1 recites, "a. *providing a structural member* having a wall means extending from a generally planar surface..." Bol emphasizes the separation of the substrate and the amorphous silicon or polysilicon layer and clearly identifies the interface 13 between the two. (Col. 3 lines 23-25). No such interface exists with a single layer substrate as found in

Applicant's invention. Given that Bol discloses a method for forming tip microstructures on a substrate using a growth mechanism applied in an additional layer, the resulting structure is not homogeneous and of necessity includes more than one layer. Thus, Bol teaches a two layer structure for building a tip microstructure. The Yeh et al. reference is directed solely to a high speed VLSI self-aligned Schottky Metal Semiconductor Field Effect Transistor (SASMESFET) *formed directly* on a silicon substrate. While Yeh teaches that the substrate may be a single crystal semi-conductor such as a silicon body or an epitaxial layer such as silicon on sapphire, the SASMESFET's are formed of layers deposited over the silicon substrate. The epitaxial layer suggested, silicon on sapphire, is a silicon-on-insulator technique. Additionally, Yeh et al. makes no mention of forming *emitter structures* directly on or integrally from a silicon substrate but instead is directed only to the formation of *SASMESFET's*. Although SASMESFET's and tip microstructures are both semiconductor devices, Applicant submits that they are substantially different in structure and purpose. Applicant respectfully submits that forming SASMESFET devices is not equivalent to forming emitters, as the devices perform different functions. These functions dictate the method of forming. While the devices may be formed in a similar fashion this does not indicate that the techniques will produce results suitable for the selected application. It would not be obvious to use a multiple layer technique to form a SASMESFET device to form a single layer emitter.

Applicant submits that the suggestion for any combination of the Bol reference and the Yeh et al. reference is based solely Applicant's disclosure, not the cited prior art. Applicant further submits that any suggestion for any combination of the cited prior art is not based upon knowledge generally available to one of ordinary skill in the art but, rather, solely upon Applicant's disclosure. Further, the mere fact that the Yeh et al. reference is incorporated by reference in the Bol reference does not indicate that it is obvious to combine or modify Bol as the has been suggested. Yeh teaches only that single-crystal semiconductor or an epitaxial layer such as silicon on sapphire may be *used for a substrate, not as a layer* in the formation of SASMESFET's. Assuming *arguendo* that a poly-silicon layer on a silicon substrate is an obvious equivalent of a silicon-on-insulator, and therefor an obvious equivalent of a semiconducting substrate, this material may be used as a substitute for the substrate in the Bol

method of forming field emitters. Substituting a poly-silicon layer on a silicon substrate for the silicon substrate in Bol would result in a first layer of amorphous silicon or polysilicon tip microstructures 22, with an interface 13 separating them from the substrate 10, a second poly-silicon layer on a silicon substrate. This combination teaches emitters formed of a separate layer on a multi-layered substrate. Therefore, the combination of Bol and Yeh et al. does not show that it is obvious to form emitters directly from a single-layered substrate. Furthermore, the Examiner has not cited a reference showing emitter structures being integrally formed from the material of a single-layered substrate. Therefore, the suggested combination of Bol and Yeh et al. is the result of impermissible hindsight based on Applicant's own disclosure.

Applicant respectfully submits that there is no reason for anyone of ordinary skill in the art to combine any teaching of the Yeh et al. reference with that of the Bol reference in the manner suggested other than Applicant's disclosure. No prior art reference has been cited in the present application that discloses forming emitter structures directly from a semiconductor substrate.

Second, Applicant submits that the proposed combination of the cited prior art of the Bol reference and the Yeh et al. reference does not teach or suggest all the claim limitations of the presently claimed invention to establish a *prima facie* case of obviousness under 35 U.S.C. § 103. Applicant respectfully disagrees with the assertion that a polysilicon layer on a silicon substrate (Bol) is an art recognized equivalent to "a single-layered substrate" (claim 23 and 27). The mere fact that Yeh et al. discloses that SASMESFET's can be formed on a silicon substrate of a single crystal semi-conductor such as a silicon body or an epitaxial layer such as silicon on sapphire does not show the equivalence of a semiconducting substrate and a poly-silicon layer on a silicon substrate. A poly-silicon layer on a silicon substrate is not the equivalent of a silicon-on-insulator, silicon on sapphire, the example given by Yeh of an epitaxial layer.

Further, regarding claim 31, even assuming *arguendo* that a poly-silicon layer on a silicon substrate is equivalent, the suggested equivalence is only for use as a substrate, with additional formation layers to be added on the substrate layer to complete the device, and not for a substrate indivisibly extending from the base of a tip. Therefore, Applicant respectfully submits that a

semiconducting substrate is not an art recognized equivalent to a poly-silicon layer on a silicon structure in for the formation of a tip.

Therefore, the cited prior art does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention.

Claims 24, 26, 28-30, and 32 are each allowable as depending, either directly or indirectly from allowable claims 23, 25, 27, and 31.

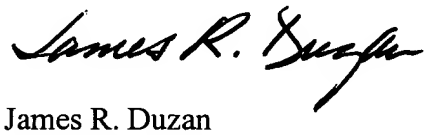
Claim 32 is additionally allowable as it recites a cathode conductor system with a dopant that defines a concentration of generally zero within a substrate. It is stated in the Office Action that it would be obvious to have a dopant gradient of zero at the base of the emitter as disclosed by Bol because the specification of the dopant gradient is within the skill of the art, as evidenced by Yeh et al. Specifying a dopant gradient provides a range of concentrations throughout the doped layer. However, this indicates dopant presence throughout the layer, not an absence of dopant. It would not be obvious to provide a region of zero doping. In fact, Yeh teaches away from a zero concentration, since Yeh teaches that dopant concentration is a variable affecting oxide bumper growth. (Col. 5, line 66 – Col. 6, line 2). Assuming that the specification of a dopant gradient is within one skilled in the art, there has been no reasoning set forth in the Office Action as to why it would be obvious to have the dopant concentration be zero or generally zero within a substrate.

CONCLUSION

For the reasons set forth hereinabove, Applicant submits that claims 23 through 32 are clearly allowable over the cited prior art.

Applicant requests the allowance of claims 23 through 32 and the case passed for issue.

Respectfully submitted,



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